Digital Systems and Microprocessors (ELE2002M)

Lab Assignment-2

Assignment Date: Thursday, 12th October 2017
Maximum Marks: 10
Due Date: Monday,, 23rd Oct 2017

Pre-requisites:

1. Learn basic Verilog Programming
2. Understand how to use and program in Vivado Design Suite (from Xilinx)
3. Learn how to create a test bench (You can write one in Verilog or else Vivado can create one for your design)

Q1. Write Verilog programs for the following Boolean logic gates and also simulate them by creating test bench for all possible input combinations. The test bench should be able to test the output for all possible input combinations. (5 marks)

(a) 2-input AND gate
(b) 3-input OR gate
(c) 2-input NAND gate
(d) 2-input NOR gate
(e) 2-input XOR gate

Q2. For the Boolean logic expression: (5 marks)

F = A'BC' + AB'C' + ABC'

a. Write a Verilog program which implements the above Boolean expression, and write a test bench to simulate it.
b. Reduce the same expression using K-map and then write a Verilog code for the reduced expression. Write the testbench and simulate the reduced expression.

Lab report must contain the following:

- The Verilog codes to all assignment questions and test benches
- Screenshots of all outputs (logic design layout and simulations)

NEXT WEEK:

1. **Learn about different data types: "wires", "nets", "registers" and "parameters". You will need to implement.**
2. **Also read about "User Constraint File (UCF)"**
3. **Read the Verilog Programming and FPGA documents available on blackboard**